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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,120	12/11/2003	Chen-Chi Kuo	P18034	7878

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EXAMINER	
CHRISS, ANDREW W	

ART UNIT	PAPER NUMBER
2609	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/733,120	KUO ET AL.	
	Examiner	Art Unit	
	Andrew Chriss	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 December 2003 and 31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892) ✓
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. **Claim 30** objected to because of the following informalities: Claim language cites "a number of packets that that have been scheduled." Claim should be amended to "a number of packets that have been scheduled." Appropriate correction is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claim 1, 3, 4, 10-15, 17, 18, 22-25, 29 and 30** rejected under 35 U.S.C. 102(b) as being anticipated by Haddock et al (United States Patent 6,104,700), hereinafter Haddock.

Regarding Claim 1, Haddock teaches selecting a QoS category with pending data (Figure 4, step 420), thus determining a packet to be transmitted via a port (Figure 1A, 105 or 110). Further, Haddock teaches determining information associated with port. Specifically, Haddock teaches a method wherein the port is polled to determine if it is ready for the next packet (Figure 4, step 410). Haddock also teaches that if the port is not ready for the next packet, the method will loop until the port is ready to receive a packet, thus preventing the packet from being placed in a transmit buffer based on the determined information (Figure 4). Lastly, Haddock teaches that the transmit buffer (any one of QoS queues 180) is associated with a plurality of ports (Figure 1A, 105 and 110).

Regarding Claim 3, Haddock teaches a CPU 130, which assists in constructing a forwarding decision for packets, thus making determinations. Haddock also teaches a packet RAM 125, which provides buffering for packets and is located externally to the CPU.

Regarding Claim 4, Haddock teaches a method wherein the information associated with the port is a port status indicating that the port is currently blocked, as a result of step 410 in Figure 4.

Regarding Claim 10, Haddock teaches a scheduler 170 that performs the process depicted in Figure 4, which includes the determination of information about a port.

Regarding Claim 11, Haddock teaches a buffer manager 165 that maintains several programmable variables for each QoS queue (column 6, lines 61-62). The buffer manager maintains a Buffers Free Count (column 7, line 9), which is incremented/decremented upon the transmission of a packet. Additionally, Haddock teaches calculating a number of packets that have been scheduled (current queue depth); and comparing the number of packets that are pending with a pre-determined threshold value (maximum queue depth).

Regarding Claim 12, Haddock teaches in step 410 in Figure 4 that if the port is not ready for the next packet, the packet is not scheduled to be transmitted, thus preventing the packet from being transmitted.

Regarding Claim 13, Haddock teaches in step 420 in Figure 4 that priority is given to the QoS category containing QoS queues with pending data that are below the peak bandwidth (column 11, lines 49-55), thus determining that a number of packets that are pending is below a pre-determined threshold. Further, Haddock also teaches scheduling the packet for transmission in step 440 in Figure 4.

Regarding Claim 14, Haddock teaches a dequeue block 162 in Figure 1B that, responsive to the scheduler 170, retrieves a packet and transmits it (column 7, lines 48-50), thus providing the packet to a transmit processing element.

Regarding Claim 15, Haddock teaches a general purpose or special purpose processor (equivalent to Applicant's claimed Article) which may have machine-executable instructions, that perform the method as described with regards to Claim 1 above.

Regarding Claim 17, see rejection of Claim 3 above.

Regarding Claim 18, see rejection of Claim 4 above.

Regarding Claim 22, Haddock teaches a dequeue block that retrieves a packet from a specified QoS queue in response to the scheduler, thus determining a packet to be transmitted from receiving a packet from a schedule processing element.

Regarding Claim 23, see rejection of Claim 10 above.

Regarding Claim 24, see rejection of Claim 11 above.

Regarding Claim 25, see rejection of Claim 12 above.

Regarding Claim 29, Haddock teaches a scheduler 170 (equivalent to Applicant's claimed schedule processing element), a CPU 130 (equivalent to Applicant's claimed transmit processing element), and a RAM 125 (equivalent to Applicant's claimed memory) external to the CPU 130. Further, Haddock teaches that the scheduler 170 prevents the packet from being provided to the transmit processing element when packets pending exceeds a pre-determined threshold value (Maximum Queue Depth) (column 7, lines 6-7).

Regarding Claim 30, teaches the scheduling processing element from the transmit process element (buffer manager 165) receiving an indication of a number of packets that have

been transmitted (peak bandwidth). Additionally, Haddock teaches the determination that the port is currently blocked is based on:

- The received indication (step 440 receiving a response that the port is not ready for the next packet);
- A number of packets that have been scheduled (current queue depth); and
- The pre-determined threshold value (maximum queue depth).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. **Claim 2, 5, 16, and 19** rejected under 35 U.S.C. 103(a) as being unpatentable over Haddock in view of Lary et al (United States Patent 5,386,514), hereinafter Lary.

Regarding Claims 2 and 16, Haddock teaches all of the limitations of Claims 1 and 15, as described above. However, Haddock does not teach a transmit buffer being a first-in, first-out

(FIFO) buffer. In the same field of endeavor, Lary teaches an insertion register, which performs a function similar to Applicant's claimed transmit buffer, wherein message entries are removed in a FIFO order (column 9, lines 51-65). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the FIFO buffer taught in Lary with the teachings of Haddock so that messages received at the transmit buffer are removed in sequence.

Regarding Claims 5 and 19, Haddock teaches all of the limitations of Claim 3 and 17, as described above. However, Haddock does not teach accessing a control status register and evaluating a bit associated with the port. In the same of endeavor, Lary teaches control/status registers (CSR) used by the port driver to convey initialization and control information to the port adapter, thus evaluating a bit associated with an individual port (column 6, lines 57-60). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the CSR taught in Lary with the teachings of Haddock in order to exchange information between the driver and the port adapter without the use of an external synchronization mechanism.

6. **Claims 6 and 20** rejected under 35 U.S.C. 103(a) as being unpatentable over Haddock in view of Lary, as applied to claims 5 and 19 above, and further in view of Vogtmeier et al (United States Patent Application Publication US 2002/0150045 A1), hereinafter Vogtmeier. Haddock and Lary teach all of the limitations of Claims 5 and 19, as described above. However, the references do not teach detecting that another packet to have been transmitted via the port was removed from the transmit buffer without being successfully transmitted. In the same field of endeavor, Vogtmeier teaches "an acknowledge signal of the transmitter consists of information

concerning the success or failure of the transmission of a single data packet, so that the response thereto is to erase the data packet from the buffer or to transmit the data packet again" (paragraph 0012). Therefore, Vogtmeier's invention is capable of detecting that a packet was removed from a transmit buffer without being successfully transmitted. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Vogtmeier with Haddock, as modified above, in order to ensure that a copy of all the data packets sent but not yet confirmed as successfully transmitted is present at the transmitter, thus preventing a loss of information.

7. **Claims 7-9, and 21** rejected under 35 U.S.C. 103(a) as being unpatentable over Haddock in view of Roach et al (United States Patent 6,005,849), hereinafter Roach.

Regarding Claims 7 and 21, Haddock teaches all of the limitations of Claims 3 and 17, as described above. However, Haddock does not teach placing the packet in a local queue stored at the transmit processing element. In the same field of endeavor, Roach teaches a full-duplex communication processor 22 (equivalent to Applicant's claimed transmit processing element) that places a packet in a local queue (transmit ready queue 60). As packets are enqueued for processing by the transmit protocol engine 32, they are thereby prevented from being placed into the transmit FIFO queue 66. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the local queue taught in Roach with the teachings of Haddock in order to perform high speed full duplex processing of data without involving the host CPU on a frame-by-frame basis.

Regarding Claim 8, Haddock does not teach determining that a port status indicates that the port is not currently blocked and arranging for the packet to be moved from the local queue

to the transmit buffer. In the same field of endeavor, Roach further teaches an NL port status unit 44, which performs the function of monitoring NL port interrupts (column 5, lines 25-27), thus providing a method for determining that a port is not currently blocked. Additionally, Roach teaches moving a packet from the transfer ready queue 60 (equivalent to Applicant's claimed local queue) to a transmit FIFO queue 66 (equivalent to Applicant's transmit buffer).

Regarding Claim 9, Haddock further teaches a dequeue block that retrieves a packet from a specified QoS queue in response to the scheduler, thus determining a packet to be transmitted from receiving a packet from a schedule processing element.

8. **Claim 31** rejected under 35 U.S.C. 103(a) as being unpatentable over Haddock in view of Berenbaum et al (United States Patent 6,272,144), hereinafter Berenbaum.

However, Haddock does not teach an ATM fabric interface device coupled to the network processor. In the same field of endeavor, Berenbaum teaches an ATM switch fabric, which connects multiple line cards (equivalent to Applicant's claimed ATM fabric interface device) of a typical ATM switch to a control processor (equivalent to Applicant's network processor). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the ATM switch fabric interface device taught in Berenbaum with Haddock in order to provide in-band device configuration and eliminate the need for a separate line card control interface.

9. **Claims 32 and 33** rejected under 35 U.S.C. 103(a) as being unpatentable over Haddock in view of Kalkunte, as applied to Claim 31 above, and further in view of Lary.

Regarding Claim 32, Haddock and Lary teach all of the limitations of Claim 31, as described above. However, the references do not teach accessing a control status register and evaluating a bit associated with the port. In the same of endeavor, Lary teaches control/status registers (CSR) used by the port driver to convey initialization and control information to the port adapter, thus evaluating a bit associated with an individual port (column 6, lines 57-60). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the CSR taught in Lary with the teachings of Haddock, as modified above, in order to exchange information between the driver and the port adapter without the use of an external synchronization mechanism.

Regarding Claim 33, Haddock further teaches a scheduler 170 (equivalent to Applicant's claimed schedule processing element), a CPU 130 (equivalent to Applicant's claimed transmit processing element), and a RAM 125 (equivalent to Applicant's claimed memory) external to the CPU 130. Further, Haddock teaches that the scheduler 170 prevents the packet from being provided to the transmit processing element when packets pending exceeds a pre-determined threshold value (Maximum Queue Depth) (column 7, lines 6-7).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Belz et al (United States Patent 6,980,552) is directed to a pipelined architecture for receiving, modifying, switching, buffering, queuing, and dequeueing packets for transmission in a communications network.

b. Tobagi et al (United States Patent 5,276,681) is directed to a process for fairly allocating resources in a multiport packet switch.

c. Kalkunte et al (United States Patent Application Publication US 2005/0018601 A1) is directed to a system to process packets received over a network

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Chriss whose telephone number is 571-272-1774. The examiner can normally be reached on Monday - Friday, 7:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on 571-270-1202. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Andrew Chriss
Examiner
Art Unit 2609

AC

CHARLES D. GARBER
SUPERVISORY PATENT EXAMINER